

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,882,579 B2
APPLICATION NO. : 10/705388
DATED : April 19, 2005
INVENTOR(S) : Brent Keeth, Brian Johnson and Troy A. Manning

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

	<u>Reads</u>	<u>Should Read</u>
On the Title Page Item (57), Line 2	"In either mode 32 bits"	--In either mode, 32 bits--
Column 1, Line 62	"or a low-speed,"	--or as low-speed,--
Column 3, Line 31	"which the"	--with the--
Column 3, Lines 44, 48, 49, 50, 52 and 53	"complimentary"	--complementary--
Column 3, Line 61	"terminals coupled serial data"	--terminals couple serial data--
Column 4, Line 3	"54 FIG. 1) includes"	--54 (FIG. 1) includes--
Column 4, Lines 4, 6, 23, 30 and 33	"complimentary"	--complementary--
Column 4, Line 50	"flip-flips 120"	--flip-flops 120--
Column 5, Line 9	"coupled twice as many"	--couple twice as many--
Column 5, Lines 39, 42 and 60	"complimentary"	--complementary--
Column 5, Line 45	"It is for this reason, that this operating"	--It is for this reason that this operating--
Column 6, Line 16	"burst of 8 bits"	--bursts of 8 bits--
Column 6, Line 34	"150a RinPar signal"	--150a a RinPar signal--
Column 6, Line 52	"signal shift the"	--signal, shift the--
Column 6, Line 61	"compliment."	--complement.--

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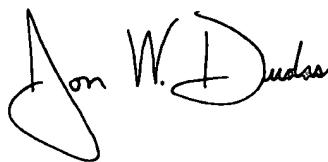
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8, Line 55	“data to or from 2N terminals of the memory device in form”	--data to or from 2N data bus terminals of the memory device in form--
Column 9, Line 9	“transferring a M*N data bits”	--transferring M*N data bits--
Column 10, Line 19	“transferring a M*N data bits”	--transferring M*N data bits--

Signed and Sealed this

Twenty-fourth Day of June, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office